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**PATENT**  
5181-94400/P6301

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.: 10/037,361  
Filed: October 29, 2001  
Inventor:  
James M. Byrd

Examiner: Gandhi, Dipakkumar B.  
Group/Art Unit: 2133  
Atty. Dkt. No: 5181-94400

Title: System and Method for  
Verifying Error  
Detection/Correction Logic

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert

Printed Name

Signature

June 21, 2005

Date

**NOTICE OF APPEAL**

**Mail Stop AF**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal to the Board of Patent Appeals and Interferences from the final rejection dated March 21, 2005 of claims 1-35.

The Commissioner is hereby authorized to charge the fee for filing this Notice of Appeal pursuant to 37 C.F.R. §1.17(e) (large entity) of \$500.00 to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5181-94400/RCK.

Respectfully submitted,

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